

Channel B IF

(637-2647-())

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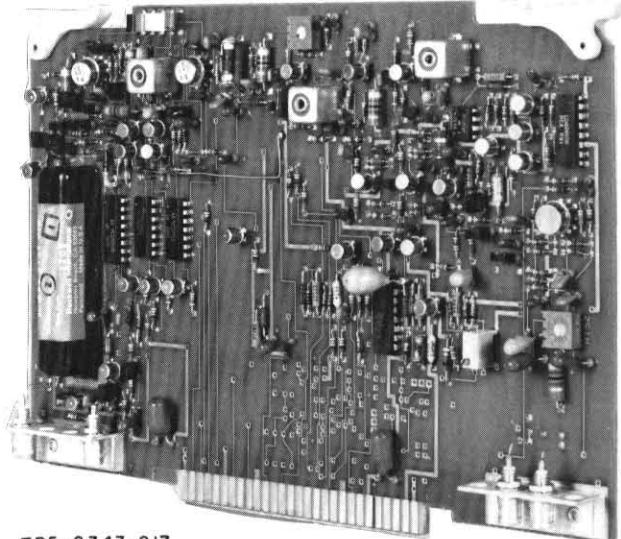


**Rockwell
International**
instructions

Collins Telecommunications Products Division

523-0767965-003211

3rd Edition, 1 January 1979



*Channel B IF
Figure 1*

2.2 Bandpass Filter Control Circuits (Refer to figure 2.)

The channel B if provides filter selection for receive if signals. Filter selection is initiated by the mode control signal, bandwidth control signal, and/or rf transmit signal. This means only that these signals are applied to the channel B if card to initiate filter selection; it does not reflect a mode of operation, selection of a bandwidth, or transmission of an rf signal.

FL2 (LSB) is selected when an FL2 (LSB) enable signal or an ISB enable and rf transmit signals are applied to the channel B if card.

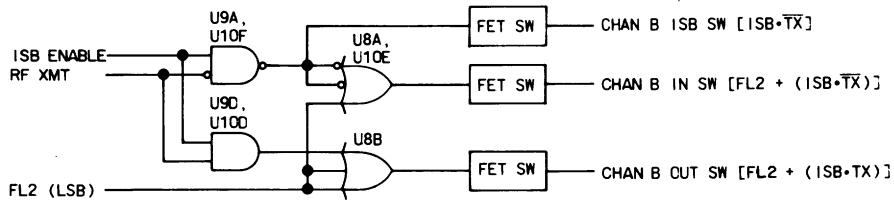
2. PRINCIPLES OF OPERATION

2.1 General

The channel B if receives the 450-kHz receive if input, filters the 450-kHz receive if signal, and provides the following:

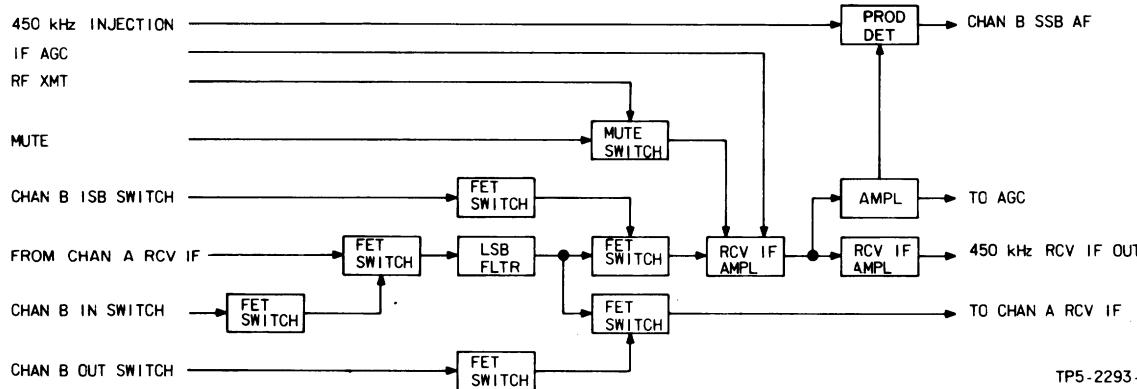
- 450-kHz receive if output
- A product-detected channel B SSB audio output
- AGC control signals

NOTICE: This section replaces second edition dated 1 June 1978.



TP5-2292-012

*Channel B Filter and IF Control Circuits
Figure 2*



TP5-2293-012

*Channel B IF Circuits
Figure 3*

2.3 Channel B IF Circuits (Refer to figure 3.)

The channel B if card receives 450-kHz receive if and supplies the 450-kHz if frequency to the LSB bandpass filter. After ISB mode or filter FL2 is selected, the 450-kHz if signal is supplied through the LSB bandpass filter. The output of the LSB bandpass filter is supplied as a channel B receive if output or is amplified and then applied as follows:

- To AGC circuits
- Through a receive if amplifier as an external 450-kHz receive if output
- Through an amplifier to a channel B SSB audio product detector. The SSB product detector receives the receive if and a 450-kHz injection, and supplies a product-detected SSB audio output.

2.4 AGC Circuits (Refer to figure 4.)

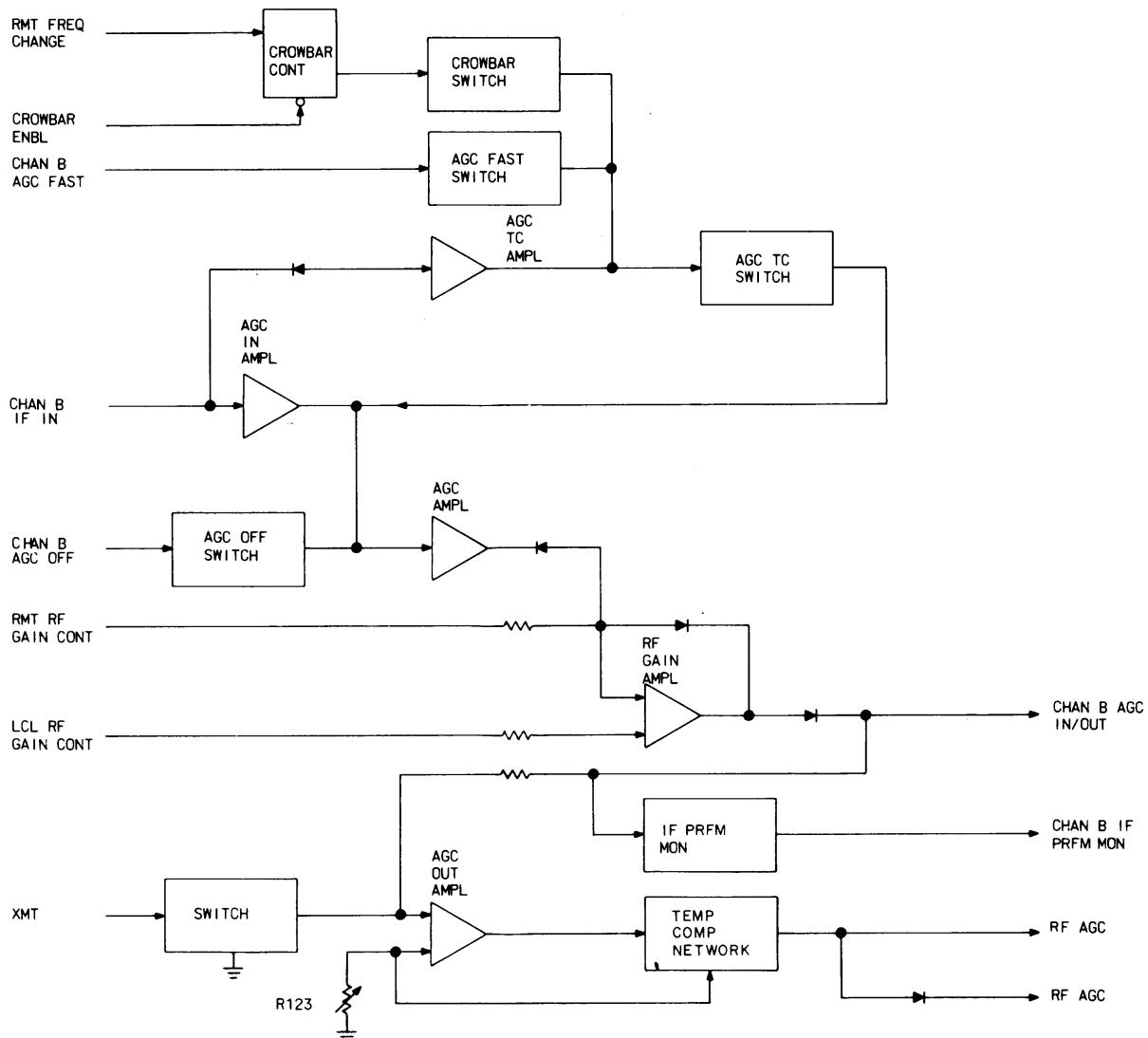
Channel B if is received by the AGC input amplifier. The AGC input amplifier and associated AGC time constant switches develop the AGC level and decay time to be used by the receiver. The AGC level is amplified and applied through rf gain amplifier, and

supplied to the if performance monitor and AGC output amplifier. The if AGC and rf AGC signals are developed and supplied to associated attenuator circuits.

With the AGC control in the SLOW position, only the AGC time constant amplifier and AGC time constant switch are enabled and establish a 1.0-second AGC decay time. (The AGC to amplifier and AGC to switch are enabled for all AGC functions.) With the AGC control in the FAST position, the AGC fast switch is enabled, reducing the time constant of the AGC circuits and establishing a 0.1-second AGC decay time. With the AGC control in the OFF position, the output of the AGC input amplifier is disabled and removed from the input of the AGC amplifier.

With the receiver in remote control and a crowbar enable applied, a remote frequency change enables the crowbar switch and reduces the AGC time constant, establishing the AGC decay time at about 2 milliseconds. The crowbar function is used for fast frequency hopping or scanning operation under processor control.

The gain of the rf gain amplifier is controlled by a local rf gain control signal. The dc voltage level



TP5-2294-013

AGC Circuits
Figure 4

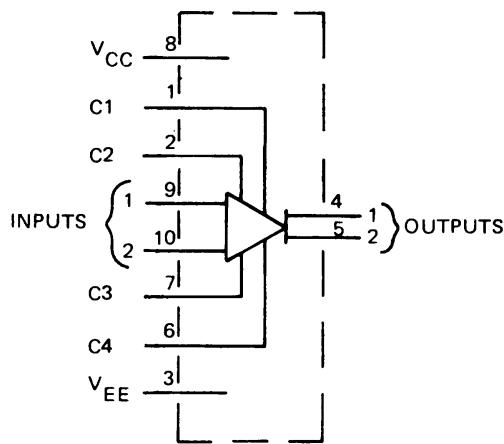
applied to the noninverting input of the rf gain amplifier establishes its gain. The remote rf gain control signal establishes the minimum gain output of the rf gain amplifier.

From the rf gain amplifier, the AGC output is supplied to channel B AGC out for use by other cards and to the channel B if performance monitor for channel B AGC indications. The rf gain amplifier output is supplied to AGC output amplifier and through AGC switch to the if/rf AGC outputs. R123 and

temperature compensating network are used to keep the if/rf AGC outputs constant throughout the frequency/temperature range.

2.5 Differential Output Operational Amplifier 351-1050-030 (Refer to figure 5.)

The 351-1050-030 is a wide-band general-purpose operational amplifier which features both differential inputs and outputs. Open loop gain is adjustable with external feedback components.



CHARACTERISTICS

SUPPLY VOLTAGE: V_{CC} +8 V DC MAX.,
V_{EE} -8 V DC MAX.

INPUT DIFF VOLTAGE: ±8 V DC MAX.

INPUT COMMON MODE VOLTAGE:
±3.0 V PEAK

INPUT RESISTANCE: 2.0 M OHM TYPICAL

OUTPUT RESISTANCE: 50 OHM TYPICAL

OPEN LOOP GAIN: SINGLE ENDED—
750 V/V MIN, 1500 V/V TYPICAL;
DIFFERENTIAL — 1500 V/V MIN.,
3000 V/V TYPICAL

BANDWIDTH: OPEN LOOP—2.0 MHz TYPICAL;
CLOSED LOOP —10.0 MHz TYPICAL

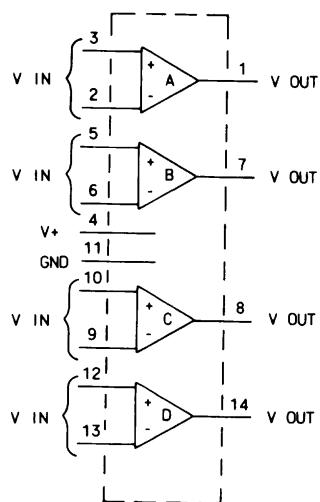
TP5-2282-011

Differential Output Operational Amplifier 351-1050-030
Figure 5

2.6 Quad Operational Amplifier 351-1141-030 (Refer to figure 6.)

The 351-1141-030 consists of four independent, high-gain, internally frequency-compensated operational

amplifiers that are designed to operate from a single power supply over a wide range of voltages. Common applications include transducer amplifiers, dc gain blocks, and all conventional operational amplifier circuits.



CHARACTERISTICS

SUPPLY VOLTAGE (V+): 32 V DC MAX

INPUT DIFF VOLTAGE: 32 V DC MAX

INPUT COMMON MODE VOLTAGE: V+ (-1.5 V DC)

OUTPUT SHORT CIRCUIT DURATION:

CONTINUOUS $\frac{1}{2}$

VOLTAGE GAIN: 25 MIN

NOTE:

① SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

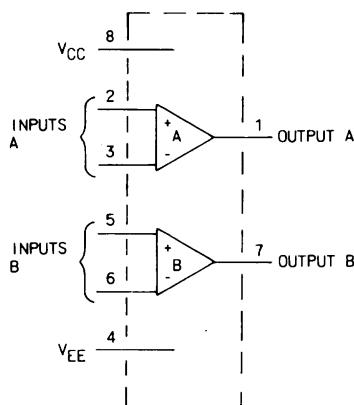
TP5-2289-013

Quad Operational Amplifier 351-1141-030
Figure 6

2.7 Dual Operational Amplifier 351-1071-070

(Refer to figure 7.)

The 351-1071-070 consists of two operational amplifiers in one package, designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components.



2.8 Dual Monostable Multivibrator 351-8278-010

(Refer to figure 8.)

The 351-8278-010 is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X .

CHARACTERISTICS

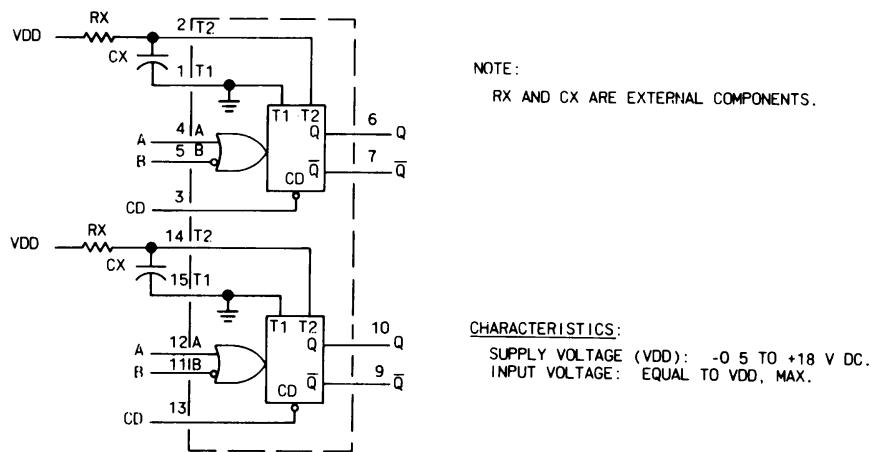
SUPPLY VOLTAGE: V_{CC} +18 V DC MAX
 V_{EE} -18 V DC MAX
INPUT DIFF VOLTAGE: ± 30 V MAX
INPUT COMMON MODE VOLTAGE:
 ± 15 V MAX (1)
OUTPUT SHORT CIRCUIT DURATION:
CONTINUOUS (2)
INPUT RESISTANCE: 300 k Ω MIN, 2.0 M Ω MAX
OUTPUT RESISTANCE: 75 Ω TYPICAL
VOLTAGE GAIN: 15 MIN

NOTES:

- (1) FOR SUPPLY VOLTAGE LESS THAN ± 15.0 V, MAX INPUT VOLTAGE EQUAL TO SUPPLY VOLTAGE.
(2) SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

TP5-2285-013

Dual Operational Amplifier 351-1071-070
Figure 7



CHARACTERISTICS:
SUPPLY VOLTAGE (VDD): -0.5 TO +18 V DC.
INPUT VOLTAGE: EQUAL TO VDD, MAX.

CHARACTERISTIC	VDD		
	5.0 V DC	10.0 V DC	15.0 V DC
OUTPUT VOLTAGE ("0" "1")	0.05 V DC MAX. 4.95 V DC MIN.	0.05 V DC MAX. 9.95 V DC MIN.	0.05 V DC MAX. 14.95 V DC MIN.
INPUT VOLTAGE ("0" "1")	2.25 V DC MAX. 2.75 V DC MIN.	4.50 V DC MAX. 5.50 V DC MIN.	6.75 V DC MAX. 8.25 V DC MIN.
EXTERNAL TIMING (RX CX)	1000 Ω MIN. NO LIMITS	1000 Ω MIN. NO LIMITS	1000 Ω MIN. NO LIMITS

TP5-2290-013

Dual Monostable Multivibrator 351-8278-010
Figure 8

2.9 Balanced Modulator-Demodulator 351-0043-020 (Refer to figure 9.)

The 351-0043-020 is designed for use where the output voltage is a product of an input voltage (signal) and a switching function carrier. Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications.

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the channel B if card are

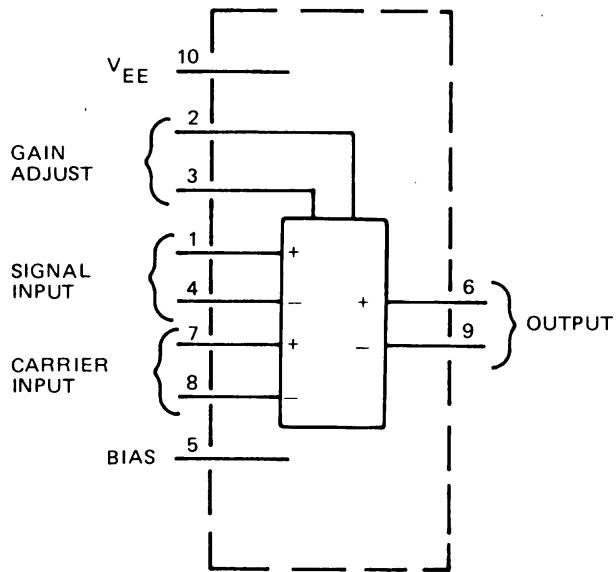
listed in the maintenance section of this instruction book.

3.2 Testing

Test procedures in table 1 check total performance of the channel B if card. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

Note

In emergencies, Channel B IF 637-2647-() can be replaced by Channel B IF 635-0902-(). In this type of repair, use the test procedures given in table 1 to test Channel B IF 635-0902-().



CHARACTERISTICS

APPLIED VOLTAGE: 30 V DC MAX PIN-TO-IN.

DIFFERENTIAL INPUT VOLTAGE: ± 5 V DC MAX

CARRIER SUPPRESSION: 65 dB TYPICAL AT 0.5 MHz; 50 dB TYPICAL AT 10 MHz.

TRANSADMITTANCE BANDWIDTH:
CARRIER INPUT—300 MHz TYPICAL;
SIGNAL INPUT—80 MHz TYPICAL

SINGLE-ENDED INPUT RESISTANCE (SIGNAL INPUT): 200 k OHM TYPICAL (AT 5.0 MHz)

SINGLE-ENDED INPUT RESISTANCE (SIGNAL INPUT): 40 k OHM TYPICAL (AT 10 MHz)

DIFFERENTIAL OUTPUT VOLTAGE SWING:
8.0 V P-P TYPICAL

TP5-2291-011

Balanced Modulator-Demodulator 351-0043-020
Figure 9

Table 1. Channel B IF, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	<p>a. Remove top cover of unit containing the channel B if that is to be tested.</p> <p>b. Remove channel A or channel B if (as noted by particular test step). Install it on an extender card and place it in the unit.</p> <p>c. Set unit LINE SELECTOR switch 115 V.</p> <p>d. Connect unit to 115-V ac power source and set power on.</p> <p>e. Measure dc voltages (on channel B if) between the following pins and ground (TP1, brown):</p> <p>P1-23 and P1-51 P1-27 P1-6</p> <p>Note Unless otherwise specified, all rf signal levels applied at J2, receive if in, are referenced to 50 Ω.</p>	+15 ±1.0 V dc +5 ±0.5 V dc -15 ±1.0 V dc	Check associated power supply.
2. FL2 (LSB) filter and ISB enable	<p>Note Channel B if card extended.</p> <p>a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to A.</p> <p>b. Measure dc voltage at the following test points to ground (TP1, brown):</p> <p>TP3 (orange) TP4 (yellow)</p> <p>c. Set front panel BANDWIDTH switch to LSB.</p> <p>d. Measure dc voltage at the following test points to ground:</p> <p>TP3 TP4</p> <p>e. Apply a +5.0-V dc signal at P1-41.</p> <p>f. Measure dc voltage at the following test points to ground:</p> <p>TP3 TP4</p> <p>g. Remove +5.0-V dc signal from P1-41.</p> <p>h. Set front panel MODE switch to ISB.</p> <p>i. Measure dc voltage at the following test points to ground:</p> <p>TP2 (red) TP3 (orange)</p>	-9.5 ±1.0 V dc -9.5 ±1.0 V dc NMT 0.5 V dc NMT 0.5 V dc NMT 0.5 V dc -9.5 ±1.0 V dc. NMT 0.5 V dc -9.5 ±1.0 V dc	Proceed to step m. Proceed to step n. Proceed to step n. Proceed to step o.
(Cont)			

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	TP4 (yellow) TP5 (green) j. Apply a +5.0-V dc signal at P1-41. k. Measure dc voltage at the following test points to ground. TP2 -9.5 ±1.0 V dc TP3 NMT 0.5 V dc TP4 -9.5 ±1.0 V dc TP5 NLT +3.0 V dc l. Remove P1-41 +5.0 V dc signal. FL2 (LSB) ENABLE AND ISB ENABLE TESTING COMPLETE	NMT 0.5 V dc NMT 0.5 V dc -9.5 ±1.0 V dc NMT 0.5 V dc -9.5 ±1.0 V dc NLT +3.0 V dc	Proceed to step p.
	TROUBLESHOOTING		
	m. Measure dc voltage at the following pins to ground: P1-42 P1-44 P1-41	NMT 0.5 V dc NMT 0.5 V dc NMT 0.5 V dc If all voltages in step m are normal, check U9, U10, U8, and Q28 (for TP3) or Q27 (for TP4).	Check FL2 (LSB) enable input circuit. Check ISB enable input circuit. Check rf transmit input circuit.
	n. Measure dc voltage at P1-42 to ground. o. Measure dc voltage at the following pins to ground: P1-42 P1-44 P1-41	NLT +3.0 V dc. Check U8 and Q28 (for TP3) or Q27 (for TP4).	Check FL2 (LSB) enable input circuit.
(Cont)		NMT 0.5 V dc NLT +3.0 V dc NMT 0.5 V dc If all voltages in step o are normal, check U9 and Q30 (for TP2); U9, U10,	Check FL2 (LSB) enable input circuit. Check ISB enable input circuit. Check rf transmit input circuit.

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	<p>p. Measure dc voltage at the following pins to ground:</p> <p>P1-42 P1-44 P1-41</p>	and U8 (for TP3 or TP4); and U10 (for TP5). NMT 0.5 V dc NLT +3.0 V dc NLT +3.0 V dc If all voltages in step p are normal, check U9 and Q30 (for TP2); U9, U10, and U8 (for TP3 or TP4); and U10 (for TP5).	Check FL2 (LSB enable input circuit). Check ISB enable input circuit. Check rf transmit input circuit.
3. 2.75-kHz LSB filter measurement	<p>Note</p> <p>This test applies only to 2.75-kHz LSB filter (526-9956-010).</p> <p>Channel A if card extended.</p> <p>a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to LSB.</p> <p>b. Set AGC switch to OFF.</p> <p>c. Set receive input to channel A if (A8J2) at 9.4517 MHz.</p> <p>d. Using an rf voltmeter, measure rf voltage at J1 (A8J4). Adjust receive input level and frequency for a 70-mV peak reading at J1 (A8J4).</p> <p>e. Adjust input frequency up until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.</p> <p>f. Adjust input frequency down until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.</p>	Reference NLT 9.453 000 MHz NMT 9.450 250 MHz	Check FL2, Q3, Q4, Q5, Q6, and associated circuits. Check FL2, Q3, Q4, Q5, Q6, and associated circuits.
3A. 3.05-kHz LSB filter measurement (Cont)	<p>Note</p> <p>This test applies only to 3.05-kHz LSB filter (526-9981-010).</p> <p>Channel A if card extended.</p>		

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3A. (Cont)	<p>a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to LSB.</p> <p>b. Set AGC switch to OFF.</p> <p>c. Set receive input to channel A if (A8J2) at 9.4518 MHz.</p> <p>d. Using an rf voltmeter, measure rf voltage at J1 (A8J4). Adjust receive input level and frequency for a 70-mV peak reading at J1 (A8J4).</p> <p>e. Adjust input frequency up until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.</p> <p>f. Adjust input frequency down until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.</p>	<p>Reference</p> <p>NLT 9.453 300 MHz</p> <p>NMT 9.450 250 MHz</p>	<p>Check FL2, Q3, Q4, Q5, Q6, and associated circuits.</p> <p>Check FL2, Q3, Q4, Q5, Q6, and associated circuits.</p>
3B. 3.10-kHz LSB filter measurement	<p>Note</p> <p>This test applies only to 3.10-kHz LSB filter (526-9986-010).</p> <p>Channel A if card extended.</p> <p>a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to LSB.</p> <p>b. Set AGC switch to OFF.</p> <p>c. Set receive input to channel A if (A8J2) at 9.4518 MHz.</p> <p>d. Using an rf voltmeter, measure rf voltage at J1 (A8J4). Adjust receive input level and frequency for a 70-mV peak reading at J1 (A8J4).</p> <p>e. Adjust input frequency up until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.</p> <p>f. Adjust input frequency down until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.</p>	<p>Reference</p> <p>NLT 9.453 400 MHz</p> <p>NMT 9.450 300 MHz</p>	<p>Check FL2, Q3, Q4, Q5, Q6, and associated circuits.</p> <p>Check FL2, Q3, Q4, Q5, Q6, and associated circuits.</p>
3C. 5.80-kHz LSB filter measurement (Cont)	<p>Note</p> <p>This test applies only to 5.80-kHz LSB filter (526-9977-010).</p> <p>Channel A if card extended.</p> <p>a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to LSB.</p>		

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3C. (Cont)	<p>b. Set AGC switch to OFF.</p> <p>c. Set receive input to channel A if (A8J2) at 9.4541 MHz.</p> <p>d. Using an rf voltmeter, measure rf voltage at J1 (A8J4). Adjust receive input level and frequency for a 70-mV peak reading at J1 (A8J4).</p> <p>e. Adjust input frequency up until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.</p> <p>f. Adjust input frequency down until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.</p>	<p>Reference</p> <p>NLT 9.456 000 MHz</p> <p>NMT 9.450 200 MHz</p>	<p>Check FL2, Q3, Q4, Q5, Q6, and associated circuits.</p> <p>Check FL2, Q3, Q4, Q5, Q6, and associated circuits.</p>
4. AGC attack and decay times	<p>Note</p> <p>Channel A if card extended.</p> <p>a. Set front panel MODE switch to ISB.</p> <p>b. Set receive input to channel A if (A8J2) at 9.4517 MHz and 1 mV at output of switching device. Set the switching device for 0.25 s on and 2.5 s off.</p> <p>Note</p> <p>If a switching device is not available, one may be fabricated using figure 10.</p> <p>c. Set front panel AGC switch to FAST.</p> <p>d. Using an oscilloscope, measure AGC attack time at Q19-C (connect test lead to Q19-C and reinstall channel B if in unit).</p> <p>Note</p> <p>AGC attack time is the time interval from the first appearance of an rf burst to the point where the rf envelope stays within 6 dB of the final value.</p> <p>e. Set receive input to channel A if (A8J2) at 9.4517 MHz and 200 μV at output of switching device. Set the switching device to alternate between a 200-μV output and a 10-μV output.</p>	NMT 5 ms	

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont.).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
	<p>f. Using an oscilloscope, measure AGC decay time at Q19-C.</p> <p style="text-align: center;">Note</p> <p>AGC decay time is the time interval from 200-μV to 10-μV transition and the point when the rf envelope reaches 70% of the final value.</p> <p>g. Repeat steps e and f with the front panel AGC switch at SLOW.</p>	75 to 200 ms 1 to 2 s	Check Q22, Q24, U4, and associated circuits. Check U4 and associated circuits.
5. 450-kHz injection frequency suppression	<p style="text-align: center;">Note</p> <p>Channel A if card extended.</p> <p>a. Set receive input to channel A if (A8J2) at 9.4517 MHz and 1000 μV.</p> <p>b. Set AGC switch to FAST.</p> <p>c. Set front panel MODE switch to ISB.</p> <p>d. Using a spectrum analyzer, measure the desired if out at J6 (CH B IF jack on rear panel).</p> <p>e. Measure the 450-kHz injection frequency leakage at the receive if out jack J6 (CH B IF jack on rear panel).</p>	Note level. NLT 40 dB down from receive if above. <p style="text-align: center;">Note</p> <p>It may be necessary to remove the receive input to locate the 450-kHz leakage. Measure it with the receive input applied.</p>	Check U1, Q1, and associated circuits.
6. Receive audio distortion	<p style="text-align: center;">Note</p> <p>Channel A if card extended.</p> <p>a. Set receive input to channel A if (A8J2) at 9.4517 MHz and 500 μV.</p> <p>b. Set front panel MODE switch to ISB.</p> <p>c. Using an audio distortion analyzer, measure the audio distortion at RCV AF 600 Ω-B on rear panel (TB1-4, -6).</p>	NMT 0.5%	Check U7, U2, U3, Q12, Q18, Q19, and associated circuits.

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. AGC range	<p style="text-align: center;">Note</p> <p>Channel A if card extended.</p> <p>a. Set front panel MODE switch to ISB.</p> <p>b. Set AGC switch to FAST.</p> <p>c. Set receive input to channel A if (A8J2) at 9.4517 MHz and 0 μV.</p> <p>d. Connect dvm to P1-21 (TB1-9 on rear panel).</p> <p>e. Increase receive input until dvm just begins to increase from 70 mV dc.</p> <p>f. Using an rf voltmeter, note rf level at J6 (CH B IF jack on rear panel).</p> <p>g. Increase receive input 80 dB higher than the input level notes in step e.</p> <p>h. Note the rf level at J6 (CH B IF jack on rear panel) and that no sign of an overload exists on Q19-C.</p>	Note input level at this point. (Nominally 5 μ V rms) Reference NMT 6 dB above that noted in step f. No overload on Q19-C.	Check U2, U3, and associated circuits.
8. Remote rf gain	<p style="text-align: center;">Note</p> <p>This test applies only to unit with a remote control connected.</p> <p>Channel A if card extended.</p> <p>a. Set receive input to channel A if (A8J2) at 9.4517 MHz and 5 μV.</p> <p>b. Set front panel CONT switch to REM.</p> <p>c. Set remote control MODE switch to ISB.</p> <p>d. Set remote control AGC switch off.</p> <p>e. Adjust remote control RF GAIN control full counterclockwise. Increase receive input at A8J2 until if output level equals reference of step c.</p> <p>f. Set receive input for 60 dB above 5-μV input. Adjust remote control RF GAIN control until if output level equals reference of step c.</p> <p>g. Note the input at P1-11 (A8P1-11).</p> <p>h. Set front panel CONT switch to LCL.</p>	Reference if output level at J6 (CH B IF jack on rear panel). Total attenuation over RF GAIN control range minimum 80 dB -5.0 - 0.1 V dc	Check U4 and associated circuits. Same as step e.

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

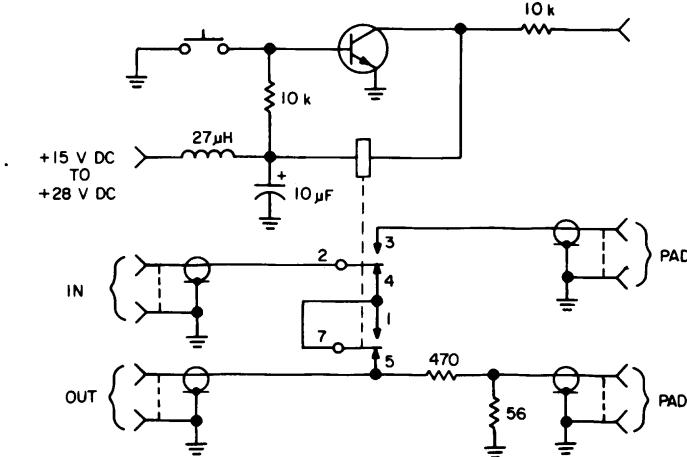
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
9. Local rf gain	<p>Note</p> <p>Channel A if card extended.</p> <ul style="list-style-type: none"> a. Set receive input to channel A if (A8J2) at 9.4517 MHz and 5 μV. b. Set front panel MODE switch to ISB. c. Set front panel AGC switch to OFF. d. Adjust front panel RF GAIN control full counterclockwise. Increase receive input at A8J2 until if output level equals reference of step b. e. Set receive input for 60 dB above 5-μV input. Adjust RF GAIN control until if output level equals reference of step b. f. Note the input at P1-39 (A8P1-39). 	<p>Reference if output level at J6 (CH B IF jack on rear panel).</p> <p>Total attenuation over RF GAIN control range minimum 80 dB</p> <p>+2.8 \pm0.3 V dc</p>	<p>Check U4 and associated circuits.</p> <p>Same as step d.</p>
10. AGC in/out	<p>Note</p> <p>Channel A if card extended.</p> <ul style="list-style-type: none"> a. Set the front panel MODE switch to ISB. b. Set front panel AGC switch to FAST. c. Set receive input to channel A if (A8J2) at 9.4517 MHz and 5 μV. d. Check the AGC in/out voltage at P1-21 (TB1-9 on rear panel) with this input applied. e. Increase the receive input to channel A if (A8J2) by 80 dB. f. Check the AGC in/out voltage at P1-21 (TB1-9 on rear panel) with this input applied. 	<p>\approx70 mV dc</p> <p>7.8 \pm0.8 V dc</p>	<p>Check U4B and associated circuits.</p> <p>Same as step e.</p>
11. Rf AGC (Cont)	<p>Note</p> <p>Channel A if card extended.</p> <ul style="list-style-type: none"> a. Set the front panel MODE switch to ISB. b. Set front panel AGC switch to FAST. c. Set receive input to channel A if (A8J2) at 9.4517 MHz and 5 μV. 	Reference	

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
11. (Cont)	<p>d. Using a dvm, monitor the rf AGC voltage at P1-18 (A8P1-18).</p> <p>e. Adjust front panel RF GAIN control for 0 V dc at P1-18 (A8P1-18).</p> <p>f. Note the rf AGC voltage while slowly increasing the receive input to 80 dB above level in step c.</p>	Rf AGC increases at a constant rate from 0 to 3 V dc. (60-dB point = NLT 3.0 V dc)	Check Q20, U4A, U4B, and associated circuits.
12. Mute	<p>Note</p> <p>Channel A if card extended.</p> <p>a. Set the front panel MODE switch to ISB.</p> <p>b. Set receive input to channel A if (A8J2) at 9.4517 MHz and 50 μV.</p> <p>c. Using an rf voltmeter, monitor the if output at J6 (CH B IF jack on rear panel).</p> <p>d. Apply a ground at P1-13 (A8P1-13).</p> <p>e. Remove P1-13 (A8P1-13) ground.</p>	<p>Output signal is present.</p> <p>Output signal is muted.</p> <p>Output signal is restored.</p>	<p>Check U2, U3, and associated circuits.</p> <p>Check Q8 thru Q11 and associated circuits.</p>
13. Performance monitor	<p>Note</p> <p>Channel A if card and parallel input card extended.</p> <p>a. Set the front panel MODE switch to ISB.</p> <p>b. Set receive input to channel A if (A8J2) at 9.4517 MHz and 50 μV.</p> <p>c. Using a dvm, measure the dc voltage at P1-2 (A11P1-18).</p> <p>d. Remove receive input and measure the dc voltage at P1-2 (A11P1-18).</p>	<p>0.5 \pm0.5 V dc</p> <p>+4.5 \pm0.5 V dc</p>	<p>Check Q25 and associated circuits.</p> <p>Same as step c.</p>
14. Crowbar enable (Cont)	<p>Note</p> <p>Channel B if card extended.</p> <p>a. Set the front panel CONT switch to REM.</p> <p>b. Apply +5 V dc to P1-37.</p> <p>c. Using an oscilloscope, monitor the waveform at U6-7.</p>	NLT +3.0 V dc	Check U6 and associated circuits.

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont.).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
14. (Cont)	<p>d. Note dc level and duration of U6-7 pulse while slowly changing the remote control frequency settings.</p> <p>e. Using an oscilloscope, monitor the waveform at P1-18.</p> <p>f. Remove +5 V dc from P1-37.</p> <p>g. Set the front panel CONT switch to LCL.</p>	<p>0.5 ± 0.5 V dc for 20 ± 10 ms between each frequency change.</p> <p>During the logic 0 pulse, waveform at P1-18 shall be 0.5 ± 0.5 V dc</p>	<p>Same as step b.</p> <p>Check Q24 and associated circuits.</p>
15. Sensitivity	<p>Note</p> <p>Channel A if card extended.</p> <p>a. Set the front panel MODE switch to ISB.</p> <p>b. Set AGC switch to OFF.</p> <p>c. Using an audio voltmeter, monitor the audio at P1-34 (A6TP8) (with no receive input).</p> <p>d. Set receive input to channel A if (A8J2) at 9.4517 MHz.</p> <p>e. Adjust receive input for -10 dB (s/n)/n at P1-34 (A6TP8).</p> <p>f. Note the receive input level.</p>	NMT 1 µV rms (into 50-Ω, 2-µV rms open circuit)	Check U2, U3, and associated circuits.
16. If output	<p>Note</p> <p>Channel A if card extended.</p> <p>a. Set the front panel MODE switch to ISB.</p> <p>b. Set receive input to channel A if (A8J2) at 9.4517 MHz and 15 µV.</p> <p>c. Set front panel AGC switch to FAST.</p> <p>d. Using an rf voltmeter, measure the receive if output at J6 (CH B IF jack on rear panel).</p>	27 ± 10 mV rms.	Check U2, U3, and associated circuits.



TPA -1345 -013

*AGC Switching Device
Figure 10*

4. ALIGNMENT/ADJUSTMENT

4.1 Filter Gain Adjustments (Selection of R29 and R41)

- Set front panel MODE switch to ISB. Set AGC switch to FAST.
- Connect receive input of 9.4517 MHz to channel A if J2.

Note

Select values of R29 and R41 only if Q3, Q5, and/or FL2 circuits have been repaired.

- Set receive signal to 50 μV (9.4517 MHz). Find a passband reponse minimum between 9.4507 and 9.4511 MHz at J1. Measure voltage gain between J4 and J1. Should be 8.2 ± 2.0 dB. Select values of R29 and R41 (200 thru 1000 Ω) to give a voltage gain of 8.2 ± 2.0 dB.

4.2 Receive Gain Adjustment (Adjustment of L5, L7, R68, and R123)

- Set front panel MODE switch to ISB. Adjust R68 for minimum gain (full ccw). Adjust receive input until channel B if output (measured at J6) indicates about 20 mV rms.
- Adjust L5 and L7 for a peak channel B if output. Decrease the receive input as necessary to maintain channel B if output at 20 mV rms.
- Repeat step b until no further increase in channel B if output is possible.
- Set the receive input to 5 μV (9.4517 MHz) and adjust R68 for $+70 \pm 5$ -mV dc AGC voltage (measured at P1-21).
- Increase receive input to 5.0 mV (9.4517 MHz) and adjust R123 until AGC voltage (measured at P1-21) equals $+5.0 \pm 0.1$ V dc.
- Repeat steps d and e until no further improvement is possible.

4.3 SSB Output Level Adjustment (Adjustment of R152)

- a. Set front panel MODE switch to ISB.
- b. Set receive input for 15.0 μ V (9.4517 MHz) and adjust R152 for 10 \pm 0.5-mV rms audio output (measured at P1-34).

5. REPAIR

Repair of the channel B if card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts and in maintenance of equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figures 11 and 12.) The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use reference designator indicated on the schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description is listed for each reference designator.

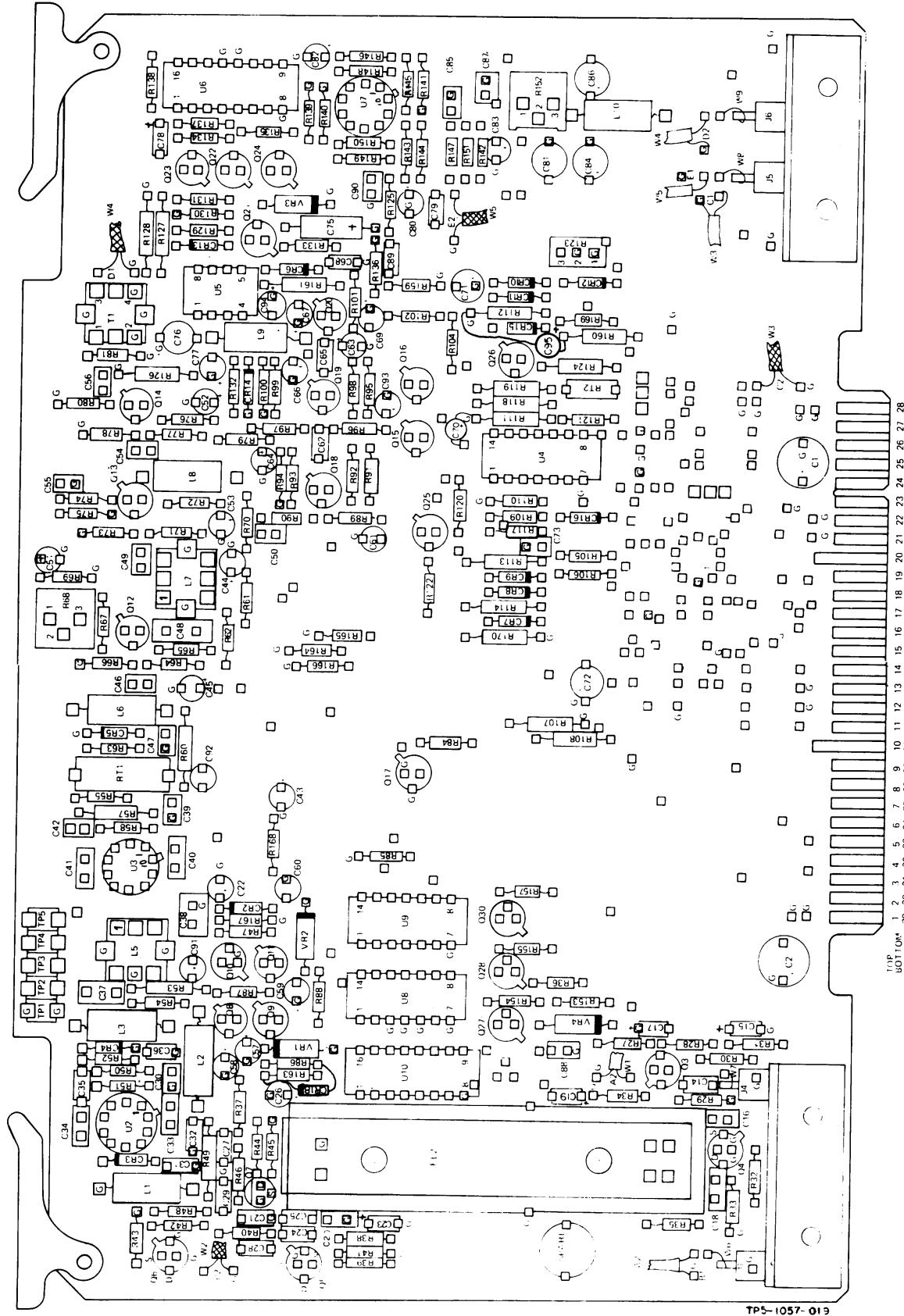
Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Channel B if	637-2647-001	REV U
Channel B if	637-2647-002	REV U
Channel B if	637-2647-003	REV U
Channel B if	637-2647-004	*

* Not covered in this printing.

Channel B IF, Through REV T, Schematic Diagram
Figure 11 (Sheet 1 of 5)



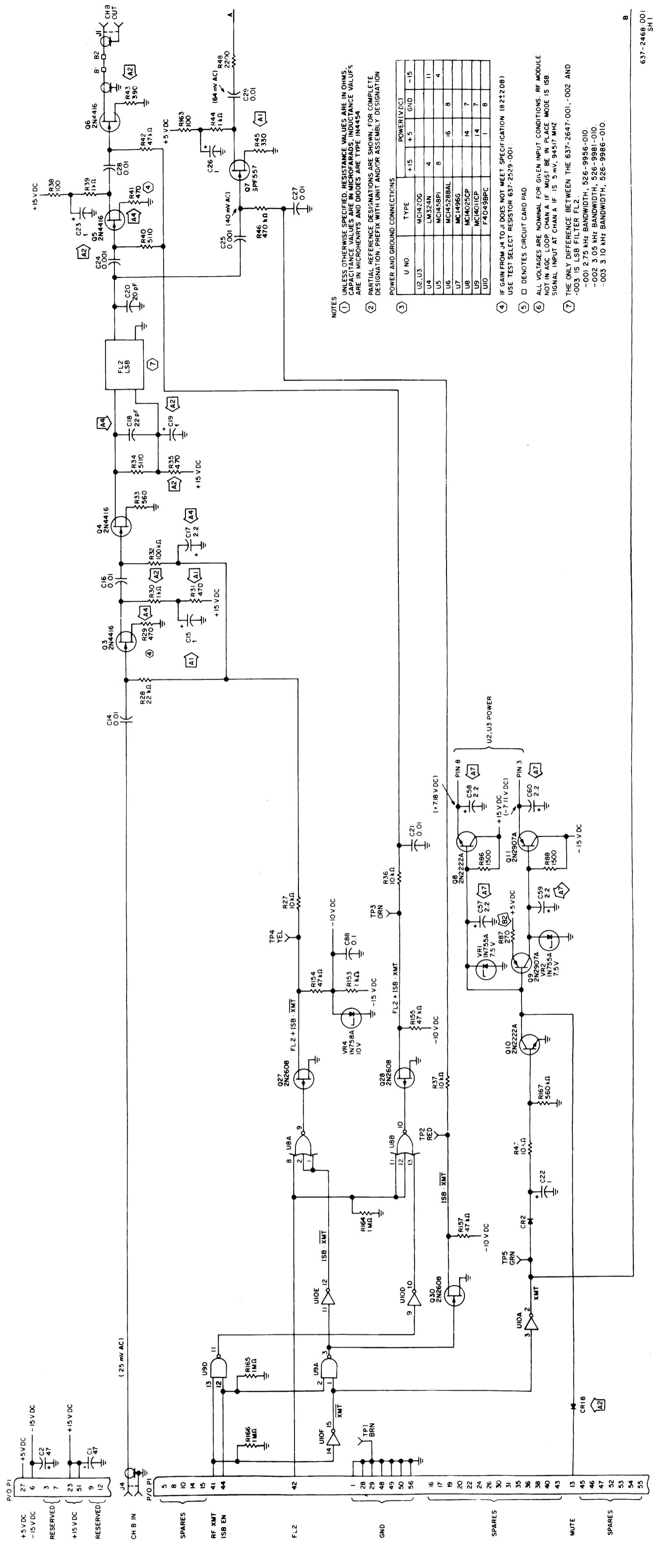
TP5-1057-019

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28
29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56

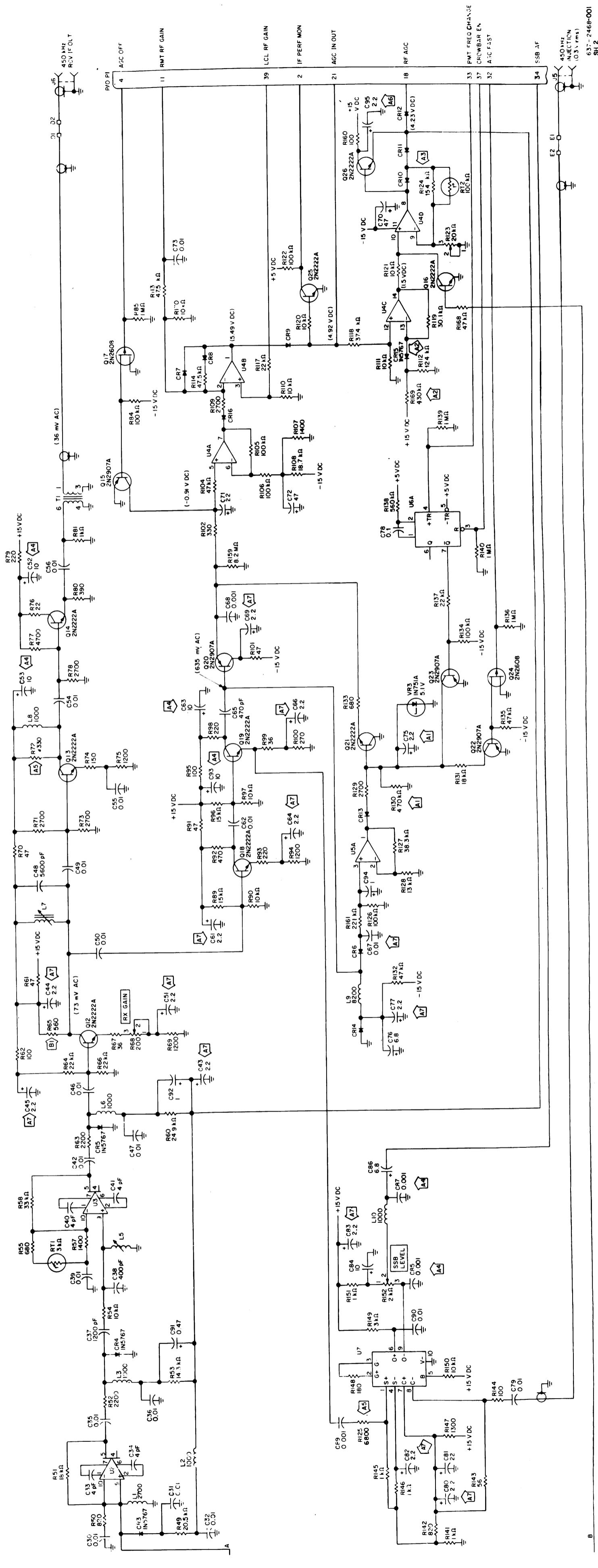
INSTRUCTIONS 523-0767965

PARTS LIST

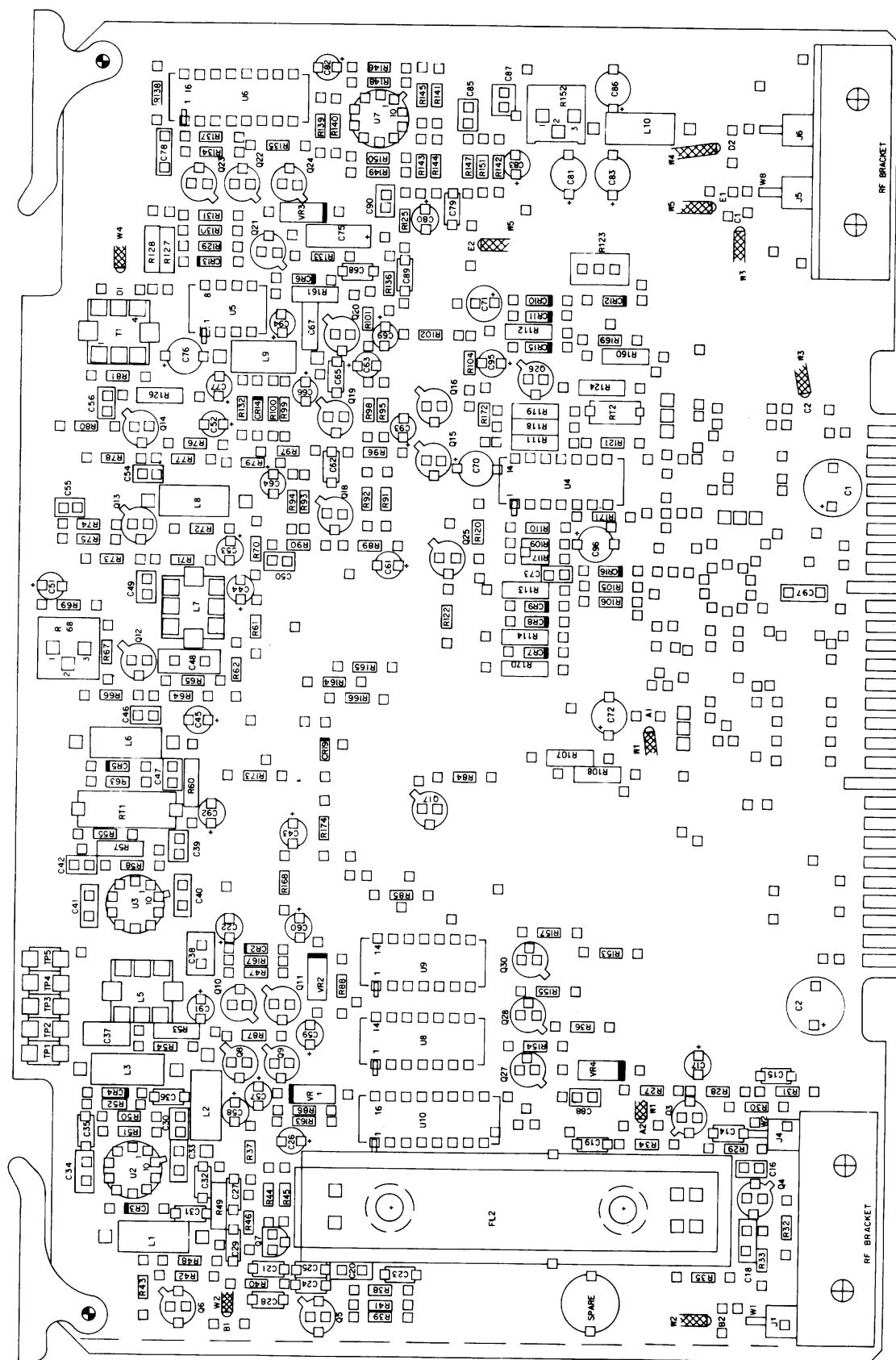
REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE	REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
C1	CHANNEL B IF A7	637-2647-001 A		C85	CAPACITOR, F2D CER DIEL, 1000PF, 10%, 20V	913-4018-000	
	CHANNEL B IF A7	637-2647-002 B		C86	CAPACITOR, F2D ELCLTY, 6.8UF, 20%, 25V	184-9102-670	
C1	NOT USED			C87	CAPACITOR, F2D CER DIEL, 1000PF, 10%, 20V	913-4018-000	
C1	SILICONIC DEVICE IN4454	353-3444-010		C88	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 50V (A4)	913-3579-110	
C1	SILICONIC DEVICE IN5167	922-6119-010		C89	CAPACITOR, F2D CER DIEL, 1000PF, 10%, 20V	913-4018-000	
C1	SILICONIC DEVICE IN5167	353-3644-010		C90	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 50V	913-3579-110	
C1	SILICONIC DEVICE IN5167	353-2564-000		C91	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 50V	184-9102-350	
C1	SILICONIC DEVICE IN5167	922-6119-010		C92	CAPACITOR, F2D ELCLTY, 1UF, 20%, 35V	184-9102-350	
C1	NOT USED	353-3644-010		C93	CAPACITOR, F2D ELCLTY, 1UF, 20%, 35V (A4)	184-9102-350	
C1	SILICONIC DEVICE IN4454	353-3444-010		C94	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 50V	913-3579-110	
C1	CAPACITOR, F2D CER DIEL, 470UF, 20%, 20V	184-9102-670		C95	CAPACITOR, F2D ELCLTY, 2.2UF, 20%, 25V (A6)	184-9102-650	
C1	NOT USED	184-9102-670		C96	CAPACITOR, F2D ELCLTY, 2.2UF, 20%, 25V	184-9102-220	
C1	CAPACITOR, F2D CER DIEL, 0.01UF, 10%, 100V	913-5019-200		C101	RESISTOR, F2D CHPSN, 100 OHMS, 10%, 1/8W	R100	
C1	CAPACITOR, F2D CER DIEL, 0.01UF, 10%, 100V (A1)	913-5019-200		C102	FILTER, L5B, 3.05 KHZ	FL2	
C1	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	184-9102-350		C103	FILTER, L5B, 3.10 KHZ	FL2	
C1	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V (A4)	184-9102-350		C104	INDUCTOR, RF 100UH	J1	
C1	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	912-4141-150		C105	INDUCTOR, RF 100UH	J2, J3	
C1	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	912-4141-150		C106	CONNECTOR, RCTP ELEC	J4-J6	
C1	CAPACITOR, F2D CER DIEL, 0.01UF, 10%, 100V	913-5019-200		C107	COIL, RF 100UH	L1	
C1	CAPACITOR, F2D CER DIEL, 0.01UF, 10%, 100V	913-5019-200		C108	COIL, RF 100UH	L2, L3	
C2	CAPACITOR, F2D CER DIEL, 0.01UF, 10%, 100V	913-5019-200		C109	NOT USED	R102	
C2	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	184-9102-350		C110	INDUCTOR, RF 100UH	R104	
C2	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	912-4141-150		C111	INDUCTOR, RF 100UH	R112	
C2	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	912-4141-150		C112	RESISTOR, F2D CHPSN, 270 OHMS, 10%, 1/8W	R113	
C2	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V (A4)	912-4141-150		C113	RESISTOR, F2D FILM, 47 OHMS, 10%, 1/8W	R114	
C2	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	184-9102-350		C114	NOT USED	R115	
C2	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	912-4141-150		C115	RESISTOR, F2D CHPSN, 330 OHMS, 10%, 1/8W	R116	
C2	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	912-4141-150		C116	RESISTOR, F2D CHPSN, 560 OHMS, 10%, 1/8W	R117	
C2	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	912-4141-150		C118	RESISTOR, F2D FILM, 37.4K, 10%, 1/8W	R119	
C2	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	912-4141-150		C119	RESISTOR, F2D FILM, 30.1K, 10%, 1/8W	R120	
C2	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	912-4141-150		C120	RESISTOR, F2D CHPSN, 10K, 10%, 1/8W	R121	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C121	RESISTOR, F2D CHPSN, 15K, 10%, 1/8W	R122	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C123	RESISTOR, F2D CHPSN, 560 OHMS, 10%, 1/8W	R124	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C124	RESISTOR, F2D FILM, 37.4K, 10%, 1/8W	R125	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C125	RESISTOR, F2D FILM, 30.1K, 10%, 1/8W	R126	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C127	RESISTOR, F2D CHPSN, 10K, 10%, 1/8W	R128	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C129	RESISTOR, F2D CHPSN, 15K, 10%, 1/8W	R130	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C130	TRANSISTOR, 2N2907A	Q30	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C131	TRANSISTOR, 2N2222A	Q11	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C132	TRANSISTOR, 2N2222A	Q11-Q14	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C133	TRANSISTOR, 2N2907A	Q15	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C134	TRANSISTOR, 2N2222A	Q16	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C135	TRANSISTOR, 2N2222A	Q17	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C136	TRANSISTOR, 2N2222A	Q18	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C137	TRANSISTOR, 2N2222A	Q19	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C138	TRANSISTOR, 2N2222A	Q20	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C139	TRANSISTOR, 2N2222A	Q21	
C3	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C140	TRANSISTOR, 2N2222A	Q22	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C141	RESISTOR, F2D CHPSN, 2.7K, 10%, 1/8W	R129	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C142	RESISTOR, F2D FILM, 1.40K, 10%, 1/8W	R130	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C143	RESISTOR, F2D CHPSN, 2.7K, 10%, 1/8W	R131	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C144	RESISTOR, F2D FILM, 1.40K, 10%, 1/8W	R132	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C145	RESISTOR, F2D CHPSN, 2.7K, 10%, 1/8W	R133	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C146	RESISTOR, F2D FILM, 1.40K, 10%, 1/8W	R134	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C147	RESISTOR, F2D CHPSN, 2.7K, 10%, 1/8W	R135	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C148	RESISTOR, F2D FILM, 1.40K, 10%, 1/8W	R136	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C149	RESISTOR, F2D CHPSN, 2.7K, 10%, 1/8W (A3)	R137	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C150	RESISTOR, F2D FILM, 1.40K, 10%, 1/8W (A3)	R138	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C151	RESISTOR, F2D CHPSN, 6.8K, 10%, 1/8W (A5)	R139	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C152	RESISTOR, F2D FILM, 6.8K, 10%, 1/8W	R140	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C153	RESISTOR, F2D CHPSN, 6.8K, 10%, 1/8W	R141	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C154	RESISTOR, F2D FILM, 6.8K, 10%, 1/8W	R142	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C155	RESISTOR, F2D CHPSN, 2.7K, 10%, 1/8W (A1)	R143	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C156	RESISTOR, F2D FILM, 1.40K, 10%, 1/8W	R144	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C157	RESISTOR, F2D CHPSN, 2.7K, 10%, 1/8W	R145	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C158	RESISTOR, F2D FILM, 1.40K, 10%, 1/8W	R146	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C159	RESISTOR, F2D CHPSN, 2.7K, 10%, 1/8W	R147	
C4	CAPACITOR, F2D CER DIEL, 0.01UF, 20%, 35V	913-5019-200		C16			



MODIFICATION HISTORY		
REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Changed: C15 from 0.01 μ F to 1 μ F. C75 from 4.7 μ F to 2.2 μ F. R3 from 100 Ω to 470 Ω . R45 from 880 Ω to 330 Ω . R130 from 270k Ω to 470k Ω .	REV C and above
A2	Added CR18, 1N4454. Changed: CR15 from 1N6116 to 1N5707. C19 from 0.01 μ F to 1 μ F. C23 from 0.01 μ F to 1 μ F. R30 from 560 Ω to 1k Ω . R55 from 100 Ω to 470 Ω . R43 from test select of 200 thru 880 Ω to fixed 380 Ω . R169 from 330k Ω to 430k Ω .	REV D and above
A3	Changed R124 from 22.6k Ω to 13.4k Ω .	REV E and above
A4	Changed: C17 from 0.01 μ F to 2.2 μ F. C18 from 15pF to 22pF. C52 from 1 μ F to 10 μ F. C53 from 1 μ F to 10 μ F. C83 from 1 μ F to 10 μ F. C85 from 0.01 μ F to 1000pF. C87 from 0.01 μ F to 1000pF. C88 from 1 μ F to 10 μ F. R29 from 560 Ω to 470 Ω . R41 from test select of 200 thru 880 Ω to fixed 470 Ω .	REV F and above
A5	Changed: R72 from 470 Ω to 330 Ω . R128 from 10k Ω to 8800 Ω .	REV J and above.
A6	Added C95, 2.2 μ F.	REV K and above
A7	Changed: C43 from 0.1 μ F to 2.2 μ F. C44 from 0.1 μ F to 2.2 μ F. C51 from 0.1 μ F to 2.2 μ F. C58 from 0.1 μ F to 2.2 μ F. C59 from 0.1 μ F to 2.2 μ F. C80 from 0.1 μ F to 2.2 μ F. C81 from 0.1 μ F to 2.2 μ F. C84 from 0.1 μ F to 2.2 μ F. C88 from 0.1 μ F to 2.2 μ F. C87 from 0.1 μ F to 0.01 μ F. C88 from 0.1 μ F to 2.2 μ F. C77 from 0.1 μ F to 2.2 μ F. C78 from 0.1 μ F to 0.01 μ F. C80 from 0.1 μ F to 2.2 μ F. C82 from 0.1 μ F to 2.2 μ F. C83 from 0.1 μ F to 2.2 μ F.	REV L and above
B1	Changed R65 from 1200 Ω to 560 Ω .	REV N and above.
B2	Changed R87 from 470 Ω to 270 Ω .	REV T and above.



Channel B IF, Through REV T, Schematic Diagram
Figure 11 (Sheet 5)

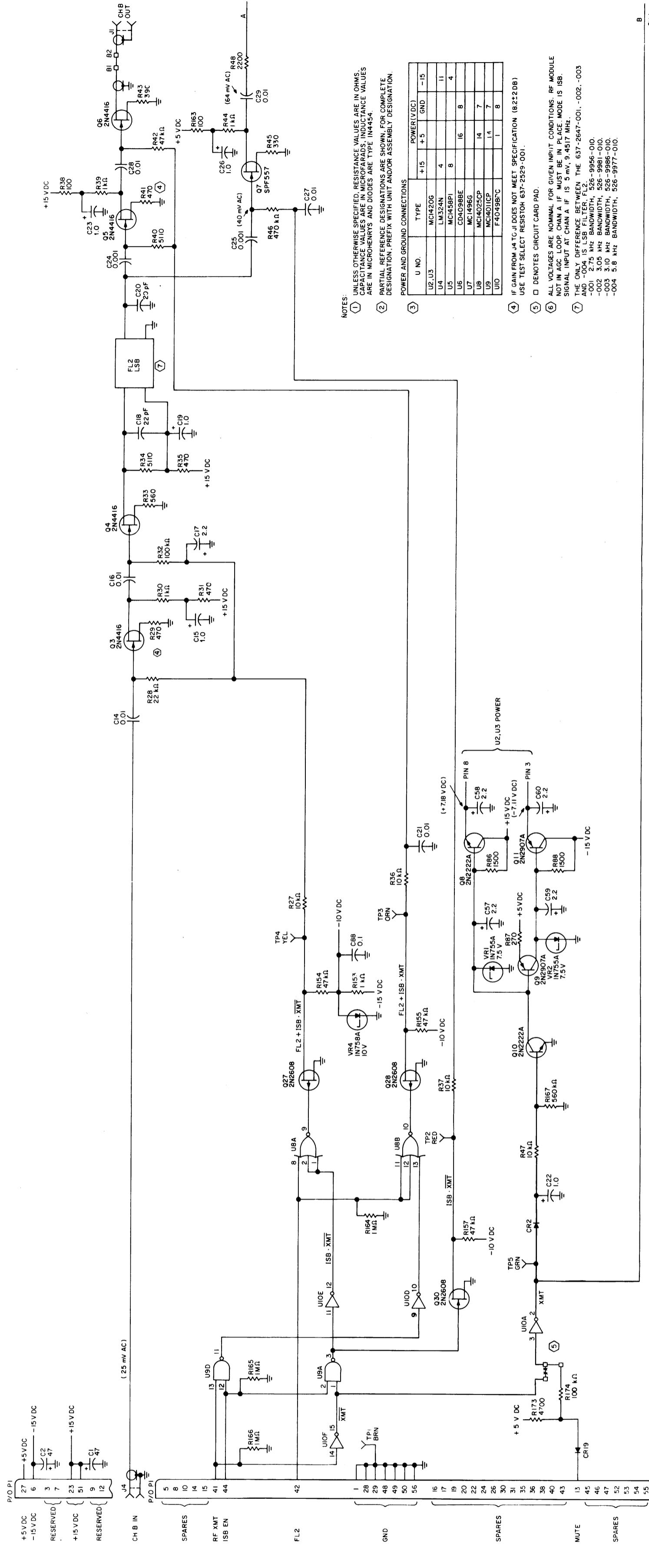


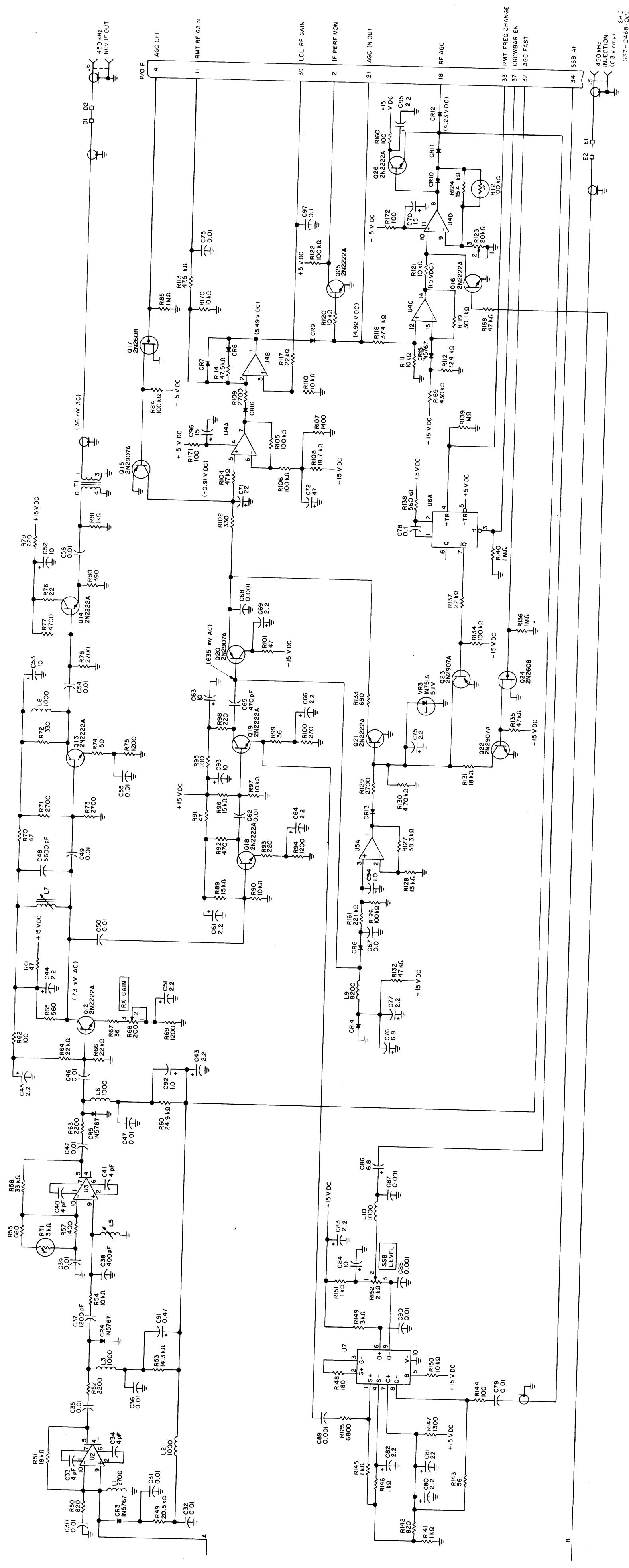
TPA-1033-018

Channel B IF, REV U and Above,
Schematic Diagram
Figure 12 (Sheet 1 of 5)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE	REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
CRI.1	NOT USED			637-2647-001 CHANNEL B IF	637-2647-002 CHANNEL B IF	637-2647-002 CHANNEL B IF	110 01,02
CRI.2	SEMICON DEVICE INN454			637-2647-003 CHANNEL B IF	353-3644-010 TRANSISTOR 2N4467	352-0756-010 TRANSISTOR 2N222A	R97 R98
CRI.3	SEMICON DEVICE INN567			353-3644-010 TRANSISTOR 2N222A	932-6119-010 TRANSISTOR 2N207A	352-0551-010 TRANSISTOR 2N222A	R99 R100
CRI.4	SEMICON DEVICE INN456			353-3644-010 TRANSISTOR 2N222A	932-6119-010 TRANSISTOR 2N207A	352-0551-010 TRANSISTOR 2N222A	R99 R101
CRI.5	SEMICON DEVICE INN567			353-3644-010 TRANSISTOR 2N222A	922-6119-011 TRANSISTOR 2N207A	352-0551-010 TRANSISTOR 2N222A	R101 R103
CRI.6	SEMICON DEVICE INN454			353-3644-010 TRANSISTOR 2N222A	912-014 TRANSISTOR 2N207A	352-0551-010 TRANSISTOR 2N222A	R115 R116
CRI.7	NOT USED			353-3644-010 TRANSISTOR 2N207A	912-014 TRANSISTOR 2N222A	352-0551-010 TRANSISTOR 2N222A	R115 R116
CRI.8	SEMICON DEVICE INN454			353-3644-010 TRANSISTOR 2N207A	912-014 TRANSISTOR 2N222A	352-0551-010 TRANSISTOR 2N222A	R117 R118
C1.1,C2	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R119 R120
C1.3	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R121 R122
C1.4	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R123 R124
C1.5	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R125 R126
C1.6	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R127 R128
C1.7	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R129 R130
C1.8	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R131 R132
C1.9	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R133 R134
C2.0	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R135 R136
C2.1	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R137 R138
C2.2,C3	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R139 R140
C2.3	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R141 R142
C2.4,C5	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R143 R144
C2.5	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R145 R146
C2.6	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R147 R148
C2.7	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R149 R150
C2.8	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R151 R152
C2.9	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R153 R154
C3.0	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R155 R156
C3.1	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R157 R158
C3.2	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R159 R160
C3.3	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R161 R162
C3.4	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R163 R164
C3.5	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R165 R166
C3.6	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R167 R168
C3.7	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R169 R170
C3.8	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R171 R172
C3.9	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R173 R174
C3.10	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R175 R176
C3.11	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R177 R178
C3.12	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R179 R180
C3.13	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R181 R182
C4.0,C4.1	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R183 R184
C4.2,C4.3	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R185 R186
C4.4	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R187 R188
C4.5	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R189 R190
C4.6	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R191 R192
C4.7	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R193 R194
C4.8	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R195 R196
C4.9	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R197 R198
C4.10	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R199 R200
C4.11	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R201 R202
C4.12	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R203 R204
C4.13	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R205 R206
C4.14	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R207 R208
C4.15	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R209 R210
C4.16	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R211 R212
C4.17	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R213 R214
C4.18	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R215 R216
C4.19	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R217 R218
C4.20	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R219 R220
C4.21	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R221 R222
C4.22,C23	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R223 R224
C4.23	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R225 R226
C4.24	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R227 R228
C4.25	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R229 R230
C4.26	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R231 R232
C4.27	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R233 R234
C4.28	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R235 R236
C4.29	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R237 R238
C4.30	CAPACITOR, F2D CER DIEI, 0.01UF, 10%, 100V	100P	20%	100P	100P	100P	R239 R240





*Channel B IF, REV U and Above,
Schematic Diagram
Figure 12 (Sheet 1)*